REMARKS

In this paper, we amended various claims. We also added claims 24-25. Presently, the application contains claims 4-5, 7-12, and 19-25.

INTERVIEW SUMMARY

On January 23, 2009, a telephonic interview was conducted between Examiner Dinh, Dan Hubert (Reg. No. 33,906) and inventor Alexander Gidon. Applicant concurs with the Examiner's interview summary set forth on form PTOL-413, dated 1-29-2009.

RESTRICTION REQUIREMENT

Previously, non-elected claims 1-3 and 13-18 were canceled in accordance with an earlier restriction requirement.

SPECIFICATION

The office action objected to the specification. The specification, as amended, overcomes the objection. The added material does not constitute new matter because features such as a computer, storage device, digital data processor, and the like are inherent to the present application as filed. The originally-filed specification, at page 1, lines 9-10, indicates that the invention relates to a "method for generating optimized timing constraint systems for retimable digital designs." For years, it has been widely known to use computer modeling to generate optimized timing constraint systems for retimable digital designs. Moreover, the specification as originally filed states "the input design 10 is expressed in a hardware description language (HDL) such as Verilog, or VHDL." [page 1, lines 14-24] The application contains numerous further references to HDL. The use of hardware description languages such as HDL invariably requires the use of a computer. The use of HDL is well documented in numerous publications, with the following being one of many examples: Computer Hardware Description Languages and Their Applications, by Dominique Borrione and Ronald Waxman, published in 1991.

Indeed, even the cited reference Selvidge recognizes the well known practice of computer modeling. "Rather than testing a logic design by programming a reconfigurable device to 'behave' as the logic device in the intended environment for the logic design, *e.g.*, the motherboard, a simulation involves modeling the logic design on a workstation." [Selvidge: col. 1, lines 40-50]

DRAWINGS

The office action objected to the drawings under 37 CFR 1.83(a). The drawings, as amended, overcome the rejection. For the same reasons explained above, the added material does not constitute new matter.

AMENDMENTS TO CLAIMS 4, 10, 11, 21-23

As this application progresses nearer to issuance, we have given additional scrutiny to all claims to prepare for allowance. In this spirit, we have amended the claims 4, 10, 11 to change the "constructing said digital circuit..." feature to "preparing a digital circuit representation..." Similar corrections were made to claims 21-23.

The construction of a physical digital circuit is unnecessary to an operation of generating timing constraints where the digital circuit, as in present example, is represented with a hardware description language. Indeed, the idea behind using hardware description languages is to perform computer modeling rather than to physically construct and physically manipulate the circuit. These claim amendments are supported by the original specification and drawings, with one example including page 1, lines 19-20. Accordingly, we have not added any new matter.

AMENDMENT TO CLAIM 7

The present amendment to claim 7 are supported by the originally filed specification and drawings. Accordingly, we have not added any new matter. Some examples of support include the following page 10 at lines 7-8), Figure 10,

page 10 at lines 10-11, Figure 11, and page 16 at line 18 through page 17 at line 15.

AMENDMENT TO CLAIM 12

We amended claim 12 to correct a technical inconsistency by changing "clock frequency" to "timing slack."

OBJECTION TO CLAIM 20

The office action objected to claim 20 for being similar to claim 4 and therefore redundant. Claim 20 has a different scope than claim 4 because, unlike claim 4, claim 20 uses "step for" language in accordance with 35 USC 112, paragraph 6. Accordingly, we kindly request the Examiner's withdrawal of the objection to claim 20.

ALLOWABLE SUBJECT MATTER

Claim 11 has been allowed. Claims 12 and 19 were cited as being allowable, subject to being rewritten as independent claims with language to overcome the section 112 issues mentioned above. Claims 12 and 19 do not need to be written, however, since the rejections to base claim 4 have been overcome, as discussed below.

NEW CLAIMS

We added new claims 24-25 in order to ensure that the application includes "computer readable storage device" and "system" counterparts to method claim 10. New claims 24-25 are is allowable for the same reason that claim 10 is allowable, as discussed above.

35 USC 103 REJECTIONS

The office action rejected claims 4-5, 7-9 under 35 USC 103 as being unpatentable over Selvidge in view of one or more of McElvain or Duggirala or Cooke. The exact patent and publication numbers of these and any later-cited

references are already stated the record. These claims, as amended, are patentably distinguished from the applied art, as explained below.

Taking claim 4 as an example, the applied references do not teach "**removing flip-flops from said digital circuit description and replacing said removed flip-flops with negative delay elements.**" Although Selvidge purportedly shows a negative delay element 1412 in Fig. 14, Selvidge does not remove a flip-flop from the circuit and replace it with a negative delay element. According to Selvidge, the latch 1410 of FIG. 14A is replaced by a flip-flop which receives the phase-advanced clock indicated by the negative delay 1412. [Selvidge: Figures 14A-14B] Rather than removing a flip flop from the circuit, Selvidge adds the flip-flop 1414 in replacement of the latch 1410. Hence, Selvidge does not teach "removing flip-flops from said digital circuit description and replacing said removed flip-flops with negative delay elements."

Claim 4 is further patentable because Selvidge does not show "**breaking any feedback paths in the digital circuit description by inserting dummy flip-flops...** " Selvidge chooses a wire 1601 in the loop and inserts a flip-flop 1602 which is clocked by the virtual clock VClk as shown in Fig. 16B. [Selvidge: col. 18, lines 55-65; Figures 16A-16B] However, Selvidge does not show a dummy flip-flop. Selvidge's FIG. 4B is said to show an exemplary timing diagram of the virtual clock signal VClk compared with a first environmental clock signal EClk1 and a second environmental clock signal EClk2. The virtual clock VClk is said to be substantially faster than any of the environmental clocks, at least four times faster but usually faster by a factor of ten to twenty. As a general rule, the temporal resolution of the virtual clock, *i.e.*, the cycle time or period of the virtual clock, should be smaller than the time difference between any pair of environmental timing signal edges. [Selvidge: col. 8, lines 5-15] However, there is nothing in Selvidge to teach or suggest that the flip-flop 1602 clocked by the virtual clock VClk is a dummy flip-flop. Indeed, Selvidge teaches that this flip-flop merely changes the timing characteristics of the loop such that "additional virtual clock cycles are required for the values in the loop to settle into their final states." [Selvidge: col. 18, lines 60-67] Therefore, Selvidge does not teach "breaking any

feedback paths in the digital circuit description by inserting dummy flip-flops... " as claimed.

Accordingly, claim 4 is patently distinguished over Selvidge. And none of McElvain or Duggirala or Cooke provide the features missing from Selvidge. The office action introduced these references merely to add an HDL context. [Office Action, page 4]

Independent claims 10 and 20-24 are allowable over Selvidge for similar reasons. As to claims 10 and 24, these are additionally patentable beyond the previous discussed reasons, because Selvidge does not show the feature "where some of the negative delay elements comprise buffers, said buffers having a load capacitance representing an average or weighted-average load capacitance taken over inputs of all gates and flip-flop D pins in a target technology library." Selvidge fails to address capacitance.

As to dependent claims 5 and 7-9, even without considering any individual merits of these dependent claims, they are allowable by virtue of their dependence on the foregoing independent claims. Nevertheless, claims 5 and 7-9 contain features that define the claims even more particularly over Selvidge.

As for claim 5, Selvidge never specifies any value for the negative delay element 1412. Therefore, Selvidge does not teach negative delay elements implemented by "buffers having a delay -T, where T is a delay equal to a flip-flop's clock period less a predetermined flip-flop delay."

As for claim 7, Selvidge chooses a wire 1601 in the loop and inserts a flip-flop 1602 which is clocked by the virtual clock VClk as shown in Fig. 16B. [Selvidge: col. 18, lines 55-65; Figures 16A-16B] However, Selvidge does not show any concern for avoiding the breakage of feedforward paths. Thus, Selvidge cannot be said to show "determining if said feedback paths can be broken without breaking any feedforward paths, where the breaking operation is conducted so as to maintain feedforward paths except where said determining operation answers in the negative."

As for claim 8, Selvidge never speaks to optimization goals and register distribution. Therefore, Selvidge fails to address said replacing step conducted

such that "predetermined optimization goals at each gate are substantially the same as they would be if registers were already optimally distributed."

As to claim 9, Selvidge does not replace any flip-flop, as mentioned above. Further, Selvidge does not disclose the delay value for the delay element 1412. Selvidge, *a fortiori*, does not teach that a delay T is "is set to a clock period of a flip-flop being replaced."

As to claims 11-12 and 19, the office action already recognized that these claims contain allowable subject matter.

CONCLUSION

In view of the foregoing, all pending claims in the application are patentable over the applied art. We request favorable reconsideration and allowance of all claims in the application.

FEES

The Commissioner is authorized to charge any fees due to the Glenn Patent Group Deposit Account No. 07-1445, Customer No. 22862.

Respectfully Submitted,

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